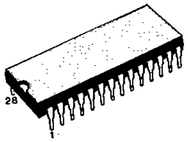
SGS-THOMSON
MICROELECTRONICS

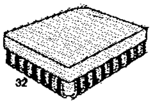
TS27C64AFN
TS27C64AP

64K (8K × 8) CMOS ONE TIME PROGRAMMABLE ROM

- COMPATIBLE TO TS27C64A EPROM (ELECTRICAL PARAMETERS, PROGRAMMING)
- PROGRAMMING VOLTAGE 12.5V
- HIGH SPEED PROGRAMMING
- 28-PIN JEDEC APPROVED PIN-OUT
- 32-PIN JEDEC APPROVED PIN-OUT (PLCC)
- IDEAL FOR AUTOMATIC INSERTION



P
DIP-28
(Plastic Package)



FN
PLCC32
(Plastic Chip Carrier)

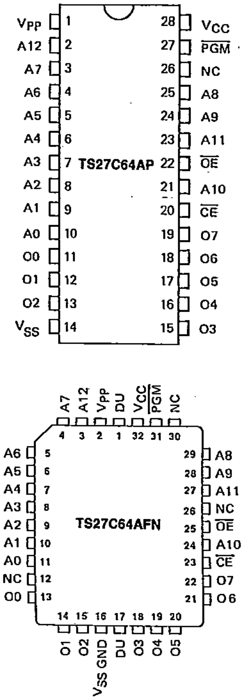
(Ordering Information at the end of the datasheet)

DESCRIPTION

The TS27C64AP and TS27C64AFN are high speed 65,536-bit One Time Programmable (OTP) CMOS ROM ideally suited for applications where fast turnaround is an important requirement.

The TS27C64AP is packaged in a 28-pin dual-in-line plastic package, the TS27C64AFN in a 32-pin PLCC plastic package and therefore can not be rewritten. Programming is performed according to standard SGS-THOMSON 64K EPROM procedure.

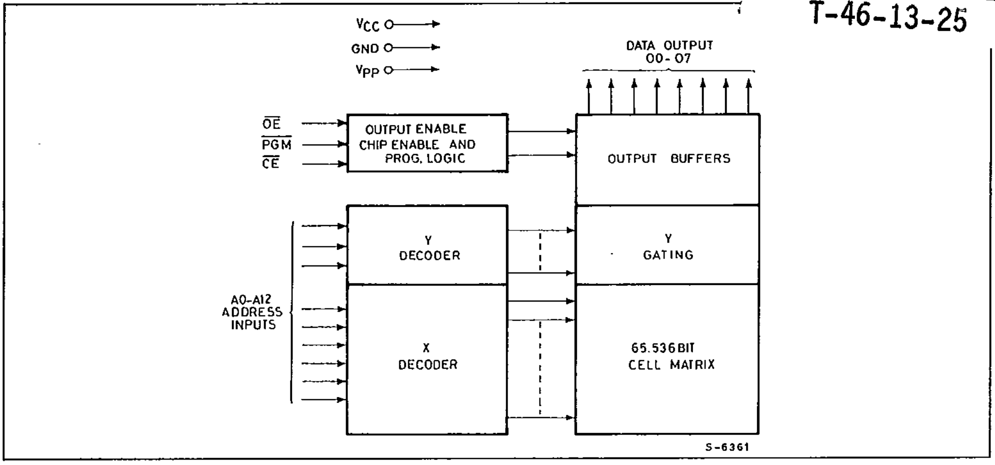
PIN CONNECTIONS



PIN NAMES

A0—A12	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NON CONNECTED
DU	DO NOT USE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range TS27C64A-C TS27C64A-V TS27C64A-T	T_L to T_H 0 to + 70 − 40 to + 85 − 40 to + 105	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C
V_{PP}(2)	Supply voltage	− 0.6 to + 14	V
V_{IN}(2)	Input voltages A9 Except V_{PP}, A9	− 0.6 to + 13.5 − 0.6 to + 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

Notes: 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND

OPERATING MODES

PINS / MODE	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	Hi-Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	CODE

Notes: 1. X can be either V_{IL} or V_{IH} — 2. $V_H = 12.0V \pm 0.5V$
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 08).

READ OPERATION

DC CHARACTERISTICS ($T_{amb} = T_L$ to T_H, $V_{CC} = 5V \pm 10\%$, GND = 0V; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.[1]	Max.	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC} - 0.7$		V_{CC}	V
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $I_{OL} = 0$ µA			0.45 0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA $I_{OH} = 0$ µA	2.4 $V_{CC} - 0.1$			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE} = \overline{OE} = V_{IL}$, Inputs $= V_{IH}$ or V_{IL}, f = 5 MHz, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE} = V_{IH}$		0.5	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE} = V_{CC}$		10	100	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{CC} = 5.5V$			100	µA

Note: 1. Typical conditions are for operation at: $T_{amb} = +25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$

AC CHARACTERISTICS[1] ($T_{amb} = T_L$ to T_H)

Symbol	Parameter	Test Conditions	27C64A -15		27C64A -20		27C64A -25		27C64A -30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		80		100		120	ns
t_{DF}[2,4]	$\overline{OE}$ or $\overline{CE}$ High to	$\overline{CE} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{OH}	Output Hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE $T_{amb} = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{out}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}•V_{PP} may be connected to V_{CC} except during program.

2. The t_{DF} compare level is determined as follows:
High to THREE-STATE, the measured V_{OH}(DC) −0.1V
Low to THREE-STATE the measured V_{OL}(DC) +0.1V.

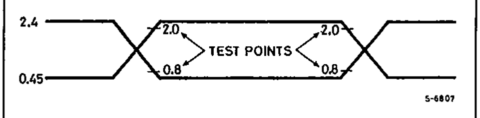
3. Capacitance is guaranteed By periodic testing. $T_{amb} = +25°C$, f = 1MHz.

4. T_{DF}, is specified from OE or CE whichever occurs first. This parameter is only sampled and not 100% tested.

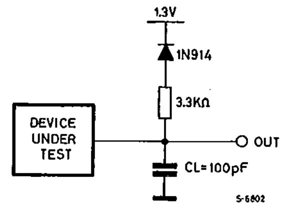
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

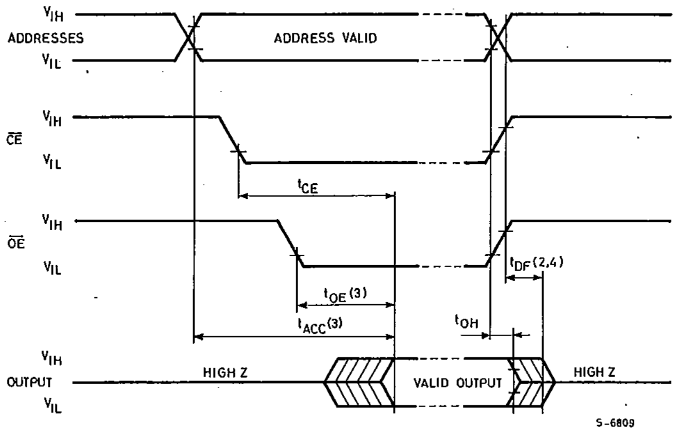


AC TESTING LOAD CIRCUIT



CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS



Notes:

1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

READ MODE

The TS27C64A has two control functions, both of wich must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to Output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C64A has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because OTPs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING

Caution: Exceeding 14V on V_{PP} pin will damage the TS27C64A.

Initially, all bits of the TS27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word.

The TS27C64A is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. It is required that a 0.1 µF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64As.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flow chart rapidly programs TS27C64A using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

PROGRAM INHIBIT

Programming of multiple TS27C64As in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64As from from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64As may be common. A TTL low-level pulse applied to a TS27C64A $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5 V will program that TS27C64A.

PROGRAM VERIFY

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5 V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will indentify the EPROM manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64A. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 of the TS27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electonic signature mode.

PROGRAMMING OPERATIONS[(1)]($T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

T-46-13-25

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (all inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -400$ μA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

S G S-THOMSON 30E D

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set-up Time		2			μs
t_{OES}	$\overline{OE}$ Set-up Time		2			μs
t_{DS}	Data Set-up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			μs
t_{VCS}	V_{CC} set-up time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}[(2)]	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{CES}	$\overline{CE}$ set-up time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

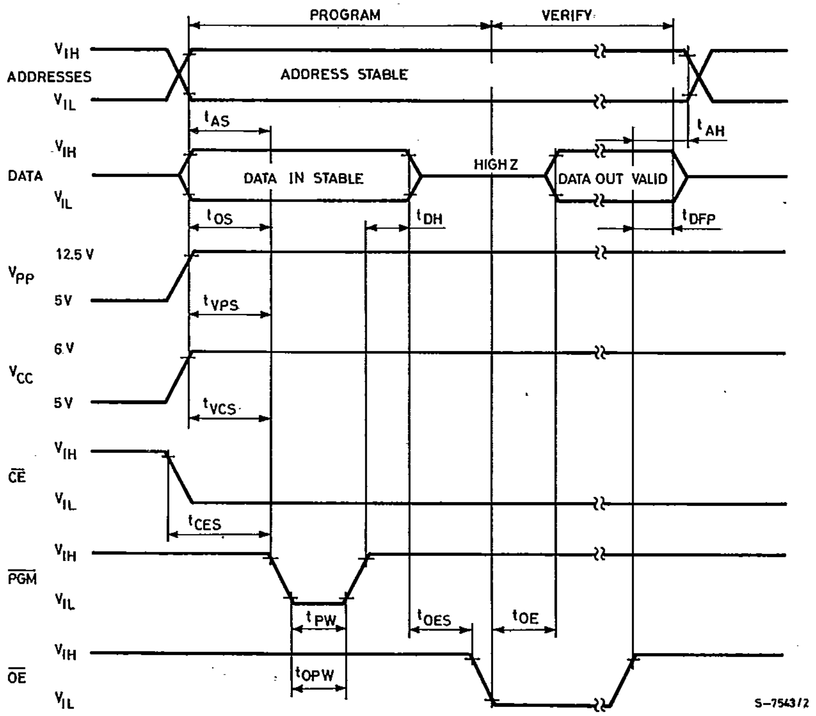
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Output timing reference level	0.8V and 2.0V

T-46-13-25

HIGH SPEED PROGRAMMING WAVEFORMS

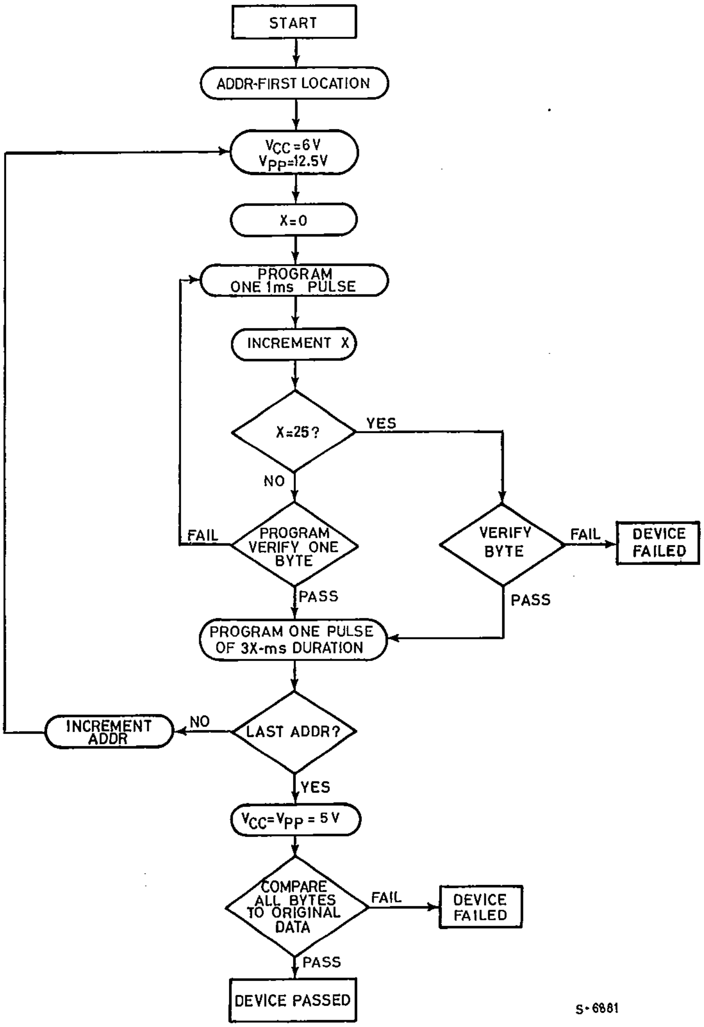
S G S-THOMSON 30E D



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be be accommodated by the programmer.
3. When programming the TS27C64A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transiens which can damage the device.

HIGH SPEED PROGRAMMING FLOW CHART

T-46-13-25

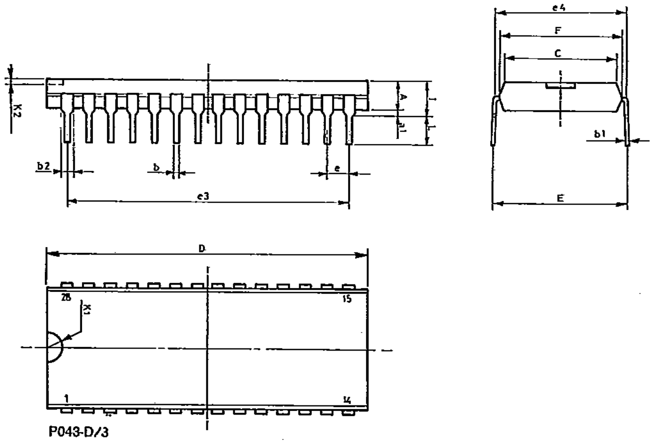


ORDERING INFORMATION (TS27C64AP) S G S-THOMSON 30E D

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-15CP	150 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-20CP	200 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-25CP	250 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-30CP	300 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-15VP	150 ns	5V ± 10%	−40 to + 85°C	DIP-28
TS27C64A-20VP	200 ns	5V ± 10%	−40 to + 85°C	DIP-28
TS27C64A-25VP	250 ns	5V ± 10%	−40 to + 85°C	DIP-28
TS27C64A-30VP	300 ns	5V ± 10%	−40 to + 85°C	DIP-28
TS27C64A-15TP	150 ns	5V ± 10%	−40 to +105°C	DIP-28
TS27C64A-20TP	200 ns	5V ± 10%	−40 to +105°C	DIP-28
TS27C64A-25TP	250 ns	5V ± 10%	−40 to +105°C	DIP-28
TS27C64A-30TP	300 ns	5V ± 10%	−40 to +105°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

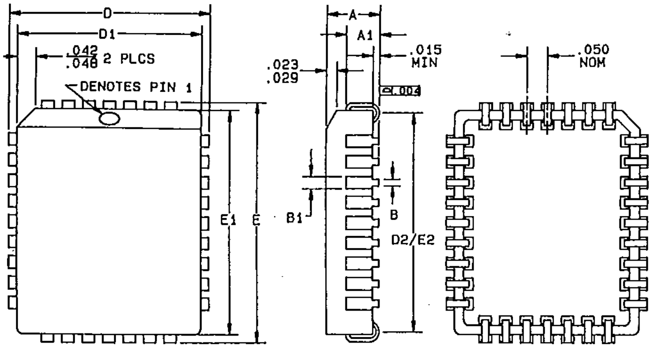
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

ORDERING INFORMATION (TS27C64AFN)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-15CFN	150 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-20CFN	200 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-25CFN	250 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-30CFN	300 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-15VFN	150 ns	5V ± 10%	−40 to + 85°C	PLCC32
TS27C64A-20VFN	200 ns	5V ± 10%	−40 to + 85°C	PLCC32
TS27C64A-25VFN	250 ns	5V ± 10%	−40 to + 85°C	PLCC32
TS27C64A-30VFN	300 ns	5V ± 10%	−40 to + 85°C	PLCC32
TS27C64A-15TFN	150 ns	5V ± 10%	−40 to +105°C	PLCC32
TS27C64A-20TFN	200 ns	5V ± 10%	−40 to +105°C	PLCC32
TS27C64A-25TFN	250 ns	5V ± 10%	−40 to +105°C	PLCC32
TS27C64A-30TFN	300 ns	5V ± 10%	−40 to +105°C	PLCC32

PACKAGE MECHANICAL DATA

PLCC32 32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm		Inches	
	Min	Max	Min	Max
A	3.04	3.55	.120	.140
A1	1.98	2.41	.078	.095
B	0.33	0.53	.013	.021
B1	0.66	0.81	.026	.032
D	12.31	12.57	.485	.495
D1	11.35	11.50	.447	.453
D2	9.90	10.92	.390	.430
E	14.85	15.11	.585	.595
E1	13.89	14.04	.547	.553
E2	12.44	13.46	.490	.530